#15 Appeal Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

12/5/02

Applicant: Terletzki, *et al.* Art Unit: 2816

Serial No.: 09/659,872 Examiner: Minh Nguyen

Filed: Sept. 13, 2000 Docket: 00-P-7882 US

For: Level-Shifting Circuitry Having "High" Output Impedance During Disable Mode

APPEAL BRIEF

Commissioner for Patents
Washington, DC 20231

Dear Sir:

This Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed June 17, 2002. A Notice of Appeal was filed on October 16, 2002 and received by the Office on October 22, 2002.

REAL PARTY OF INTEREST

The present application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals or interferences.

STATUS OF THE CLAIMS

Claims 1-5, 7-13, 15, 18, 20-28 and 30 stand finally rejected. Claim 6 has been allowed and claims 14, 16, 17, 19 and 29 are objected to as depending from a rejected claim. Claims 14 and 23 were objected to for informalities, which Appellant has addressed in the accompanying Amendment under 37 C.F.R. § 1.116. Thus, the subject matter of the instant appeal is the final rejection of Claims 1-5, 7-13, 15, 18, 20-28 and 30. These claims are reproduced in Appendix I.

STATUS OF AMENDMENTS

An amendment is being filed concurrently with this brief. This amendment addresses non-substantive issues. Appellant does not believe that this amendment has any bearing on the issues addressed in this brief.

SUMMARY OF THE INVENTION

The present invention relates to level shifting circuitry. Page 1, line 5.[1] Figure 1 shows a prior art circuit 9 that can be used to shift lower voltage signal levels to higher voltage signal levels. Page 1, line 6. The known level shifting circuit 9 receives an input logic signal IN having a first voltage level (e.g., 2.1 V) representative of a first logic state (e.g., "1") or a second voltage level (e.g., ground) representative of a second logic state (e.g., "0"). Page 1, line 13. The circuit 9 provides an output logic signal at an output terminal OUT. *See* page 1, lines 18-23. The output logic signal has a third voltage level (e.g., 2.5 V) representative of the first logic state (e.g., "1") and a fourth voltage level (e.g., ground) representative of the second logic state (e.g., "0"). *Id.*

[1] The page and line numbers refer to related portions of the application for the purpose of showing support in the originally filed paper. Appellant makes no assertion that the cited portion is the only or even the most relevant reference.

Figure 2 illustrates a first preferred embodiment of the present invention. In this preferred embodiment, the output OUT can be selectively placed in a high impedance mode based on the enable signal ENABLE. Page 4, line 4. In the high impedance mode substantially little or no current passes through the output terminal OUT. Page 4, line 6. Referring to the example of Figure 2, in this mode the output terminal OUT is isolated from the 2.5 volt level node by transistor P_3 and from the ground node by transistor N_3.

The circuit 10 includes a level shifting section 12 that is similar to the level shifting circuit of Figure 1. Page 3, line 18. The circuit 10 of the invention also includes an enable/disable section 14 coupled to the level shifting section 12 and is responsive to an enable/disable signal ENABLE. Page 3, line 19. The enable/disable section 14 places the output terminal OUT at a relatively high output impedance condition independent of the logic state of the input logic signal IN during a disable mode. Page 4, line 4. The paragraph beginning on the ninth line of page 4 describes the particular circuitry, while the operation of that circuitry is described beginning on page 5, line 4.

ISSUES

(1a) Claim 1 specifically recites an enable/disable section that places an output terminal at a relatively high output impedance condition. Can this claim be anticipated by the Stewart reference which teaches a circuit that never places an output terminal at a relatively high impedance condition?

(1b) Claims 2-5, 7-8 and 20-30 recite an enable/disable section that places an output terminal at a relatively high output impedance condition. Are these claims obvious over the Stewart reference which never places an output terminal at a relatively high impedance condition?

(2a) Claim 1 specifically recites an enable/disable section that places the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode. Can this claim be anticipated by or obvious over the Stewart reference which never teaches an output that is independent of the logic state of the input?

(2b) Claims 2-5, 7-8 and 20-30 recite an enable/disable section that places the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode. Can these claims be obvious over the Stewart reference which never teaches an output that is independent of the logic state of the input?

(3) Claims 2-5, 7-19 and 20-30 each recite a circuit that includes both a first element (e.g., transistor or other switch) between a first reference node and other circuitry and a second element (e.g., transistor or other switch) between a different reference node and the other circuitry. Are these claims obvious over the Stewart reference which teaches circuitry with either the first transistor or the second transistor but provides no suggestion or motivation to include both?

(4) Claims 3, 4, 12, 15, and 23-28 are each dependent claims that recite limitations not taught or suggested by the applied prior art. Are any of these claims obvious over the Stewart reference when the reference does not teach or suggest their respective limitations?

GROUPING OF THE CLAIMS

The groupings of claims that stand and fall together are listed below. The reasons for this grouping are clearly set forth in the arguments.

a. Claim 1 stands or falls alone.

b. Claims 2, 7 and 8 stand or fall together.

c. Claims 4 and 5 stand or fall together.

d. Claims 9, 10, 11, and 18 stand or fall together.

e. Claims 12 and 13 stand or fall together.

f. Claims 20, 21, 22, 23, 25 and 30 stand or fall together.

g. Claims 3, 15, 24, 26, 27 and 28 each stands or falls alone.

h. Claims 6, 14, 16, 17, 19, and 29 have been indicated as being allowable.

ARGUMENTS

It is respectfully submitted that claims 1-5, 7-13, 15, 18, 20-28 and 30 recite patentable subject matter under the provisions of 35 U.S.C. § 102 and 35 U.S.C. § 103.

1. The Rejection

The Examiner finally rejected claims 1 and 7-8 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,216,390 to Stewart (hereinafter "Stewart" or "the Stewart reference"). The Examiner has also finally rejected claims 2-5, 9-13, 15, 18, 20-28 and 30 under 35 U.S.C. § 103(a) as being obvious over Stewart. Since claims 7-8 depend from claim 2, Appellant will treat these rejections as if they were made under Section 103.

To save space, these rejections will not be repeated here. Relevant aspects of the rejections will be discussed in the Appellant's arguments.

2. Appellant's Arguments

Appellant respectfully submits that each of the presently pending claims is allowable over the references of record. Each of the issues indicated above will now be addressed.

(1a) Claim 1 specifically recites an enable/disable section that places an output terminal at a relatively high output impedance condition. Can this claim be anticipated by the Stewart reference which teaches a circuit that never places an output terminal at a relatively high impedance condition?

Claim 1 recites that "the enable/disable section plac[es] the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode." It is respectfully submitted that Stewart does not teach or suggest the limitations of claim 1.

The Examiner states that the Stewart reference discloses "an enable/disable section 16 coupled to the level shifting section wherein the level shifting section responsive to an enable/disable signal Vc for placing the output terminal 30 to a high output impedance condition (when transistor P3 is OFF) independent of the logic state of the input signal during disable mode." Final rejection, 6/17/02, p. 3. Applicant respectfully submits that this statement is factually incorrect.

First, the circuit taught by Stewart never places the output terminal 30 in a high impedance mode. As explained by Stewart, control circuit 16 is for selectively changing the operating potential applied to latch 12. "When V_C is at V_1, P3 is turned-on and V_3 volts are then applied to node 34. . . . When V_C is at V_3, P3 is turned-off and V_2 volts are coupled to node 34 via D2." Col. 2, lines 20-24. In other words, the reference describes two conditions for transistor P3 and in neither case is the output 34 placed at a relatively high output impedance condition. The reference

simply does not teach this limitation.

In the final rejection, the Examiner responded to this argument with three points. Each of the Examiner's points will be repeated and then discussed by Appellant. In his first argument, the Examiner stated:

> Regarding the argument that Stewart does not teach or suggest the enable/disable section places the output terminal at a relatively high output impedance condition independent of the logic state of the input signal during a disable mode. The examiner notes that as discussed in the preceding rejection, the enable/disable section reads on transistor P3 which is when an input voltage to the gate of P3 is LOW, the output terminal is at low output impedance and when the input voltage to the gate of P3 is HI, the output terminal 30 is at high output impedance independent of the logic state of the input logic signal, and the recited limitation is met. [Final rejection, 6/17/02, p. 9.]

Appellant respectfully submits that this argument is factually incorrect. As stated in the present specification, a terminal is at a high impedance condition when substantially little or no current passes through the terminal. Page 4, lines 6-8. The Stewart reference never teaches a condition when the output terminal 30 is in a high impedance condition. A high voltage condition is not the same as a high impedance condition. The state of transistor P3 only determines whether node 34 will be held at V_2 or V_3 volts. It has no effect in causing output terminal 30 to be placed in a high impedance mode.

In his second argument, the Examiner stated that:

> Regarding the argument that the reference does not teach any condition where the terminal 30 is placed at a relatively high output impedance condition. The examiner notes that the teaching is shown in Fig. 1. The Applicants are reminded that the drawings must be considered as part of the disclosure. [Final rejection, 6/17/02, pp. 9-10.]

Appellant whole-heartedly agrees that the drawings are considered part of the disclosure. This fact is inapposite. Stewart's Figure 1 simply does not teach any operation mode where the output terminal will be held at a high impedance condition. As explicitly shown in the figure itself,

output terminal 30 will be at either V_1 or V_2-V_F or V_3 volts. None of these conditions is a relatively high output impedance condition.

In this third argument, the Examiner stated that:

> Regarding the argument that the control circuit 16 is merely for selectively changing the operating potential applied to latch 12. This argument is not found persuasive because the Applicants fail to show why the claimed enable/disable circuit and the prior art enable/disable circuit both have the same structure, but the prior art circuit cannot function as the claimed circuit. In order for the argument to be persuasive, the Applicants need to show either the function of the enable/disable circuit recited in the claim resulting in different structure from the reference circuit or the prior art circuit cannot perform the function recited in the claim (MPEP 2112.02). [Final rejection, 6/17/02, p. 10.]

The function of the enable/disable circuit recited in the claim results in different structure from the reference circuit and the prior art circuit cannot perform the function recited in the claim. When transistor P3 is turned off, node 34 will be driven to V_2-V_F volts. *See* Figure 1. Stewart never teaches removing the connection between node 26 and node 34.[2] Accordingly, the prior art and the preferred embodiment do not have the same structure and the prior art circuit cannot perform the recited function.

Appellant observes that the preferred embodiment of the claimed invention (see e.g., Figure 2) and Stewart's circuit of Figure 1 both include a p-channel transistor coupled between a reference voltage node and another p-channel transistor. Appellant strongly asserts, however, that a claim cannot be anticipated simply because a prior art reference shows some of the same elements. In order for a claim to be anticipated, the prior art reference must show all of the limitations. In this case, the prior art does not teach an enable/disable section that places an output terminal at a relatively high output impedance condition.

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[2] Stewart does teach that diode D2 can be replaced with a transistor switch. Col. 2, line 13. Stewart never suggests, however, that this transistor and the transistor P3 could both be turned off, much less the specific limitations of claim 1.

Stewart does not teach all of the limitations of claim 1 and therefore cannot anticipate the claim. Since this is the only rejection of claim 1, it is respectfully submitted that claim 1 is allowable.

(1b) Claims 2-5, 7-8 and 20-30 recite an enable/disable section that places an output terminal at a relatively high output impedance condition. Are these claims obvious over the Stewart reference which never places an output terminal at a relatively high impedance condition?

Claims 2-5 and 7-8 depend from claim 1 and therefore include all of the limitations of claim 1. Claim 20 recites the limitation that "the enable/disable section caus[es] the output terminal to be placed at a relatively high output impedance condition." Claims 21-30 depend from claim 20 and therefore also include this limitation.

As shown above, Stewart does not teach or suggest an enable/disable section that causes an output terminal to be placed at a relatively high output impedance under any conditions. Appellant has clearly demonstrated that this limitation is not anticipated by the reference. Further, the Examiner has provided no rationale as to how the reference could render the limitation obvious. Appellant asserts that it does not. The reference does not teach or suggest any output terminal ever being placed in a high impedance mode, much less the specific limitations of the claims, and therefore cannot be used to invalidate the claims that include this limitation.

(2a) Claim 1 specifically recites an enable/disable section that places the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode. Can this claim be anticipated by or obvious over the Stewart reference which never teaches an output that is independent of the logic state of the input?

As discussed above with respect to Issue 1, the Stewart reference does not teach an enable/disable section that causes an output terminal to be placed at a relatively high output

impedance condition. Assuming for the sake of argument that the Examiner were correct and the transistor P3 is in fact such a circuit, Appellant respectfully submits that the reference still does not anticipate the claim because the Examiner has failed to address all of the limitations.

Claim 1 specifically recites that the enable/disable section places the output terminal "at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode" (emphasis added). The Examiner has not addressed this limitation, which is not taught or suggested any place in the Stewart reference.

Referring to Figure 1 of Stewart, when the input logic signal at node 28 (or 22) is a logical 1, the output terminal 30 will be at logic "0" (zero volts) regardless of the value of the signal V_C. This is described by Stewart in the two paragraphs starting at column 2, line 51 and ending at column 3, line 4. In the first of the two paragraphs, the transistor P3 is off (so that V_2-V_F volts are applied to node 34) and "the output 30 is clamped to zero volts." Col. 2, line 59. In the second of the two paragraphs, the transistor P3 is on and the potential at node 30 is maintained at ground potential. Col. 3, line 2.

Simply put, the state of output terminal 30 is highly dependent upon the logic state of the input logic signal. Whenever the input logic signal is a logical "1", the output terminal 30 will be held at ground (which is zero volts).

The Examiner has made no argument that contradicts this fact. Therefore, claim 1 is not anticipated by Stewart.

(2b) Claims 2-5, 7-8 and 20-30 recite an enable/disable section that places the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode. Can these claims be obvious over the Stewart reference which never teaches an output that is independent of the logic state of the input?

Claims 2-5 and 7-8 depend from claim 1 and therefore include all of the limitations of claim 1. Claim 20 recites the limitation that "the enable/disable section caus[es] the output terminal to be placed at a relatively high output impedance condition independent of the logic state of the input logic signal in response to a disable mode indication from the enable/disable signal" (emphasis added). Claims 21-30 depend from claim 20 and therefore also include this limitation.

As stated above, the prior art does not teach or suggest placing an output terminal in a relatively high impedance state independent of the logic state of the input logic signal. The Examiner has not pointed to any portion of the reference that contradicts this fact. Appellant respectfully submits that this is because the limitation is not obvious and these claims are allowable.

(3) Claims 2-5, 7-19 and 23-30 each recite a circuit that includes both a first element (e.g., transistor or other switch) between a first reference node and other circuitry and a second element (e.g., transistor or other switch) between a different reference node and the other circuitry. Are these claims obvious over the Stewart reference which teaches circuitry with either the first transistor or the second transistor but provides no suggestion or motivation to include both?

a. Claims 2-5, 7-8

Claim 2 depends from claim 1 and adds further limitations. For example, claim 2 specifically recites "an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and . . . the second one of the pair of transistors having a second electrode coupled to the fourth voltage level through the second switching transistor." The first and second switching transistors are fed by the enable/disable signal.

The Examiner concedes that Figure 1 of the Stewart reference does not explicitly teach "a second switching transistor and the second one of the pair transistor having a second electrode coupled to a source of a second voltage level through the second switching transistor." Final rejection, 6/17/02, p. 5.

The Examiner contends that:

> Stewart discloses another level shifting circuit (Fig. 3) having a second switching transistor N5A, and he further teaches that when the input logic signal swings in a negative region (column 4, line 31), i.e., the second voltage level is negative, a second switching transistor N5A should be added (column 4, lines 30-60).
>
> It would have been obvious to one skilled in the art at the time of the invention was made to include a second switching transistor taught in Fig. 3 of the Stewart reference to the Stewart's level shifting section shown in Fig. 1.
>
> The motivation/suggestion for doing so would have been to allow the Stewart's level shifting circuit shown in Fig. 1 to function when the levels of the input logic signal is either positive or negative.
>
> Therefore, it would have been obvious to add the second switching transistor to Fig. 1 of the Stewart reference to obtain the invention as specified in claim 2.

Appellant respectfully submits that the limitations of claims 2-5 and 7-8 would not be obvious in view of the prior art. The Examiner has not pointed to any suggestion within the reference that portions of two distinct circuits could be selectively combined. When applying Section 103, the prior art must be considered as a whole. MPEP § 2141. In this case, the Stewart reference never suggests that the circuits of Figures 1 and 3 be combined. In fact, as will be discussed below, a reading of the entire patent shows that the two circuits are alternatives, to be chosen between when the circuit voltage levels change.

Looking at the reference itself, Stewart never teaches or suggests a circuit that has input logic signals that are either positive or negative. The Examiner has pointed to no such suggestion and Appellant cannot find such suggestion. The circuit of Figure 3 is an alternative to that of Figure 1. In particular, Figure 1 applies in the case where the input varies from 0 V to 5 V and Figure 3

applies when the input varies from –5 V to 0 V. Col. 1, line 55, col. 4, line 30. The reference provides no suggestion that a single circuit could receive a three level (-5V, 0V, +5V) input and the reference certainly provides no indication of what the output of such a circuit would be. Since the reference does not teach or suggest the limitations, it cannot render the claim obvious.

Further, Appellant fails to see how this rationale to modify Stewart's circuits is even relevant to the issue at hand, namely whether it would be obvious to include a second switching transistor as recited in the claim. Assume, for the sake of argument, that the input logic signal can be either positive or negative. How would this lead one to include a switching transistor between one of the pair of transistors and a reference node? The final rejection provides no hint.

As a different point, claim 2 also requires that "the first and second switching transistors are fed by the enable/disable signal." Stewart does not teach or suggest that the first and second switching transistors are fed by the enable/disable signal. The Examiner states that "[t]his limitation would have been obvious also since the first and second switching transistors must be both ON or OFF during any period of time, therefore, by using only one signal, this requirement can be obtained. A further motivation would have been by using a single signal, the control section would be simpler." Final rejection, 6/17/02, pp. 5-6.

Appellant finds no support in the Stewart reference as to why the first and second switching transistors must be both ON or OFF during any period of time. First of all, Stewart never teaches a circuit that includes both first and second switching transistors. As a result, the reference cannot teach this further requirement. Even assuming that the alternate circuits of Stewart's Figure 1 and Figure 3 could somehow be combined, Appellant sees no reason why the transistors must be both ON or OFF. Frankly, it is difficult to understand the basis of this requirement. It is certainly not from the reference.

In fact, the requirement seems inconsistent with the alleged motivation to modify the circuits in the first place. Stewart teaches two circuits at issue here. In Figure 1, the output is 0 V when the input (as defined by node 22 or 28) is at 5 V (logic "1") and the output is either 5 V or 20 V when the input is at 0 V (logic "0"). In Figure 3 the output is either -5 V or -20 V when the input is at 0 V (logic "1") and the output is 0 V when the input is at –5 V (logic "0"). The Examiner states that one would be motivated to modify these circuits "to function when the levels of the input logic signal is either positive or negative." Final rejection, 6/17/02, p. 5. None of these situations seem to indicate that both switching transistors be ON.

Since the reference does not teach the limitations and since the limitations are not even remotely suggested, Appellant respectfully submits that claims 2-5 and 7-8 are allowable.

b. Claims 9-19

Claim 9 specifically recites "a second n-channel transistor having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to a second voltage level reference node and a gate coupled to a first enable signal node; [and] . . . a second p-channel transistor having a first source/drain region coupled to the second source/drain region of the first p-channel transistor, a second source/drain region coupled to a third reference node and a gate coupled to a second enable signal node." Appellant respectfully submits that the references of record do not teach or suggest the limitations of claim 9.

The Examiner rejects this claim on the same basis as the rejection of claim 2. As discussed above, Stewart provides no suggestion that the circuit of Figure 1 can be combined with the circuit of Figure 3. The prior art must be considered as a whole. In this case, the prior art includes no motivation to combine the two distinct circuits and therefore the combination is improper.

In addition, the Examiner's motivation does not seem to even lead to a circuit that would read on the claim. The stated motivation is for the circuit "to function when the levels of the input logic signal is either positive or negative." Assume that the input levels can be either –5 V, 0 V, or + 5 V, the collection of choices of the two circuits. How would this new circuit operate? What would the output be if the input was – 5 V? 0 V? 5 V? More relevant to the issue at hand, why would this lead to including the second n-channel transistor and second p-channel transistor required by claim 9?

The final rejection provides no answers to these questions. More importantly, Stewart provides no answers to these questions. Simply stated, Stewart does not teach or suggest the circuit recited by claim 9. It appears that the Examiner is improperly relying upon the teaching of Appellant's disclosure to find motivation to modify Stewart. There is no such motivation without the benefit of hindsight from Appellant's own teaching.

Further, claim 9 recites "an input node to receive an input signal, the input signal varying between a first voltage level and a second voltage level." Claim 9 also recites that the second n-channel transistor is coupled to a second voltage level and the second p-channel transistor is coupled to a third reference node carrying a third reference voltage level different than the first voltage level. The Examiner has not reconciled his hypothetical circuit with these requirements of claim 9.

Therefore, it is respectfully submitted that claim 9 is allowable over the references of record.

Claims 10-19 each depend from claim 9. Each of these dependent claims is also allowable by reason of depending from an allowable claim. Those claims that have not been indicated as standing or falling with claim 9 are discussed in more detail below.

c. Claims 20-30

Independent claim 20 specifically recites "an enable/disable section including a first portion coupled between the level shifting section and the first reference voltage node and a second portion coupled between the level shifting section and the third reference voltage node." Claims 21-30 each depend from claim 20 and therefore also include these limitations.

Similar to the statements above, Stewart does not teach or suggest a first portion and a second portion as recited by claim 20. The reference itself provides no teaching or motivation to create such a circuit.

The Examiner states that "the recited first portion reads on transistor N5A and the recited second portion reads on transistor P3 and these portions are connected as recited." Final rejection, 6/17/02, p. 8. The transistors N5A and P3, however, are found in different circuits and therefore cannot read directly on the claim. Further, the reference itself provides no motivation, much less any teaching, as to why the circuits would be combined. And finally, as discussed above, the motivation provided by the Examiner does not lead to a circuit that reads on the claim.

Therefore, it is respectfully submitted that claims 20-30 are allowable over the references of record.

(4) Claims 3, 4, 12, 15, and 23-28 are each dependent claims that recite limitations not taught or suggested by the applied prior art. Are any of these claims obvious over the Stewart reference when the reference does not teach or suggest their respective limitations?

a. Claims 3-5

Claim 3 depends from claim 2, which depends from independent claim 1. Claim 3 specifically recites that "the enable/disable section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of

the first switching transistor." Claims 4 and 5 depend from claim 3. Stewart does not teach or suggest the limitations of claims 3-5.

According to the Examiner, "the recited limitation that the enable/disable section includes an inverter is met because as shown in Fig. 1 and 3, the first switching transistor P3 is P type and the second switching transistor N5A is N type, therefore, when using only the enable/disable signal to turn ON or OFF both of these transistor, an inverter must be included." Final rejection, 6/17/02, p. 6.

The Examiner's rationale is based on ungrounded suppositions. First, Stewart makes no suggestion to use "only the enable/disable signal to turn ON or OFF both of these transistor." Stewart never even teaches these transistors in the same circuit. As discussed above, there is no basis for the requirement that both transistors are ON or OFF together. Second, the Examiner provides no explanation as to why an inverter must be included.

The conclusions drawn by the Examiner are not based on the prior art reference, as is required to reach a conclusion of obviousness. Therefore, Appellant respectfully submits that claims 3-5 are allowable over the references of record.

b. Claims 4-5

Claim 4 depends from claim 3 and further recites that "the inverter is powered by a voltage source held at the first voltage level." Claim 5 depends from claim 4 and, therefore, includes the same limitations.

The Examiner states that "since it is clear that the inverter discussed in claim 3 above must be powered by a voltage source, and the inverter can be operated when the voltage source is held at the first voltage level, the recited limitation is met." Appellant respectfully submits that this conclusory statement is insufficient as a matter of patent law to render a claim obvious.

The Examiner has not pointed to any circuit that includes both an inverter and multiple supply sources as required by the claim. More importantly, the Examiner has provided no rationale as to why the first voltage level would be used to power the inverter. Without some suggestion in the prior art, the claim is not obvious.

c. Claims 12-13

Claim 12 depends from claim 11, which depends from claim 10, which depends from claim 9. Claim 12 specifically recites "an inverter having an input and an output, the input coupled to the first enable signal node and the output coupled to the second enable signal node." Claim 13 depends from claim 12 and, therefore, includes the same limitations.

Appellant respectfully submits that the limitations of claim 12 are not taught or suggested by the references of record. The Examiner rejects this claim for the same reason noted with respect to claim 3. As discussed above with respect to claim 3, however, this rejection is not based on the teachings of any cited prior art and is grounded in unfounded supposition. Stewart does not teach any inverter much less the specific limitations of claim 12. Further, Stewart does not teach any circuit that would utilize such an inverter.

Therefore, it is respectfully submitted that claims 12 and 13 are allowable.

d. Claim 15

Claim 15 depends from independent claim 9 and specifically recites that "a signal carried at the first enable signal node is an inverted version of a signal carried at the second enable signal node." Appellant respectfully submits that this claim is allowable over the references of record.

The Examiner has rejected this claim on the basis that "since the second enable signal node receives the signal through the inverter, the recited claim limitation is met." Final rejection,

6/17/02, p. 8. Unfortunately, the Examiner has never cited any prior art that teaches or suggests an inverter. As a result, this rejection is on its face deficient.

As discussed above, the references of record do not teach or suggest an inverter. Therefore, claim 15 is allowable over the references of record.

e. Claim 24

Claim 24 depends from claim 23, which depends from claim 22, which depends from independent claim 20. Claim 24 recites that "wherein both the third and fourth transistors are rendered conductive when the enable/disable signal indicates that the level shifting circuit is in an enable mode and wherein both the third and fourth transistors are rendered non-conductive when the enable/disable signal indicates that the level shifting circuit is in the disable mode." Appellant respectfully submits that claim 24 is allowable.

The Examiner states that "the recited limitation is merely the result when the circuit is operated and since the prior art circuit discussed in claim 23 has all the recited structure, the recited limitation result is clearly met." Appellant respectfully disagrees.

First, the prior art never teaches or suggests the limitations of claim 23. Second, even if it did, the prior art certainly never teaches the specific limitations of claim 24. The Examiner seems to assume, without any basis, that if a circuit included the third and fourth transistors then both transistors would be conductive during an enable mode and non-conductive in a disable mode. This limitation certainly is not suggested by Stewart, who never mentions any disable or enable modes. The Examiner has provided no basis for the teaching of this limitation.

Therefore, it is respectfully submitted that claim 24 is allowable.

f. Claim 26

Claim 26 depends from claim 25, which depends from independent claim 20. This claim recites "an inverter coupled between a control terminal of the first switch and a control terminal of the second switch." As discussed above with respect to claim 3, however, this limitation is never taught or suggested by the prior art and therefore Appellant respectfully submits claim 26 is allowable.

g. Claim 27

Claim 27 depends from claim 26 and further recites that "the inverter includes an input coupled to the control terminal of the first switch and an output coupled to the control terminal of the second switch." As discussed above with respect to claim 3, however, this limitation is never taught or suggested by the prior art and therefore Appellant respectfully submits claim 27 is allowable.

h. Claim 28

Claim 28 depends from claim 26 and further recites that "the inverter is coupled to the third reference voltage node." Appellant respectfully submits that this claim is allowable over Stewart.

The Examiner states that this claim is rejected for the same reasons noted in claim 13, which stated it would "have been obvious also since by connecting to an existing node to receive the power source, only a single power supply is needed." Appellant respectfully submits that this statement begs the question. Claim 28 is limited to a circuit that includes at least two reference voltage nodes and claims that a very specific element (the inverter) that is connected in a very specific way (between a control terminal of a first switch and a control terminal of a second switch) and is coupled to a very specific power supply (the third reference voltage node). Appellant

respectfully submits that knowledge that inverters are connected to power supplies provides no help in suggesting that the specific inverter of claim 28 be coupled to the specific power supply of claim 28.

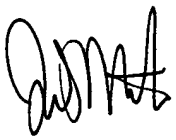
Therefore, it is respectfully submitted that claim 28 is allowable over the references of record.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the Examiner's final rejection of claims 1-5, 7-13, 15, 18, 20-28 and 30 under 35 U.S.C. § 102 and § 103 is improper and respectfully requests that the Board of Patent Appeals and Interference so find and reverse the Examiner's rejections.

To the extent necessary, the Appellant petitions for an Extension of Time under 37 C.F.R. 1.136. Please charge any fees, or credit any overpayments, in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 50-1065.

Respectfully submitted,



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APPENDIX I

ALL PENDING CLAIMS

1. (Amended) Level shifting circuitry, comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output terminal thereof having a third voltage level representative of the first logic state of the input logic signal; and a fourth voltage level representative of the second logic state of the input signal;

an enable/disable section coupled to the level shifting section, the enable/disable section being responsive to an enable/disable signal, the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode.

2. (Twice Amended) The level shifting circuitry recited in claim 1, wherein the level-shifting circuitry includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

a first switching transistor;

a second switching transistor;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting

circuitry, a control electrode of the second one of the pair of transistors being connected to the second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the fourth voltage level through the second switching transistor; and

wherein the first and second switching transistors are fed by the enable/disable signal.

3. (Amended) The level shifting circuitry recited in claim 2 wherein the enable/disable section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor.

4. (Amended) The level shifting circuitry recited in claim 3 wherein the inverter is powered by a voltage source held at the first voltage level.

5. The level shifting circuitry recited in claim 4 wherein the control electrode of the input transistor is coupled to the source of the first voltage level.

6. (Amended) Level shifting circuitry comprising:

a level-shifting section responsive to an input logic signal, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state, such level-shifting section providing an output logic signal at an output terminal thereof having a third voltage level representative of the first logic state of the input logic signal;

an enable/disable section coupled to the output terminal, the enable/disable section being responsive to an enable/disable signal, the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal

during a disable mode, the enable/disable section including a first switching transistor and a second switching transistor;

wherein the level-shifting section includes:

an input transistor having a control electrode, a first electrode coupled to the input logic signal, and a second electrode;

an output pair of serially coupled complementary type transistors, a first one of the pair of transistors having a first electrode coupled to a source of the third voltage level through the first switching transistor and a control electrode coupled to the second electrode of the input transistor, a junction between the output pair of transistors providing the output terminal for the level-shifting circuitry, a control electrode of the second one of the pair of transistors being connected to the second electrode of the input transistor, the second one of the pair of transistors having a second electrode coupled to the second voltage level through the second switching transistor;

wherein the first and second switching transistors are fed by the enable/disable signal;

wherein the enable/disable section includes an inverter, and wherein such inverter is fed by the enable/disable signal, such inverter having an output coupled to the control electrode of the first switching transistor;

wherein the inverter is powered by a source of the first voltage level; and

wherein the inverter comprises a level shifter for shifting the level of the enable/disable signal from the first voltage level to the third voltage level and for feeding such third voltage level to the control electrode of the first switching transistor to place the first switching transistor to a non-conducting condition during the disable mode.

7. (Amended) The level shifting circuitry recited in claim 2 and further comprising an additional transistor having a control electrode coupled to the junction, a first electrode coupled to the source of the third voltage level through the first switching transistor and a second electrode coupled to the second electrode of the input transistor.

8. The level shifting circuitry recited in claim 7 wherein the input transistor and the additional transistor are of opposite conductivity type.

9. A level shifting circuit comprising:

an input node to receive an input signal, the input signal varying between a first voltage level and a second voltage level;

a first n-channel transistor having a first source/drain region, a second source/drain region and a gate, the gate being coupled to the input node;

a second n-channel transistor having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to a second voltage level reference node and a gate coupled to a first enable signal node;

a first p-channel transistor having a first source/drain region coupled to the first source/drain region of the first n-channel transistor, a second source/drain region and a gate coupled to the input node;

a second p-channel transistor having a first source/drain region coupled to the second source/drain region of the first p-channel transistor, a second source/drain region coupled to a third reference node and a gate coupled to a second enable signal node, the third reference node carrying a third voltage level, the third voltage level being different than the first voltage level.

10. The circuit of claim 9 and further comprising a third n-channel transistor having a first source/drain region coupled to the input node, a second source/drain region coupled to the gate of the first p-channel transistor, and a gate coupled to a first voltage level reference node.

11. The circuit of claim 10 and further comprising a third p-channel transistor having a first source/drain region coupled to the gate of the first p-channel transistor, a second source/drain region coupled to the second source/drain region of the first p-channel transistor, and a gate coupled to the first source/drain region of the first p-channel transistor.

12. The circuit of claim 11 and further comprising an inverter having an input and an output, the input coupled to the first enable signal node and the output coupled to the second enable signal node.

13. The circuit of claim 12 wherein the inverter comprises:

a fourth n-channel transistor with a first source/drain region coupled to the second enable signal node, a second source/drain region coupled to the first voltage level reference node, and a gate coupled to the first enable signal node;

a fourth p-channel transistor with a first source/drain region coupled to the second enable signal node, a second source/drain region coupled to the third reference voltage node, and a gate coupled to the first enable signal node.

14. The circuit of claim 13 wherein the inverter further comprises:

a fifth n-channel transistor with a first source drain region coupled to the first enable signal node, a second source/drain region coupled to gate of the fourth p-channel transistor, and a gate coupled to the first voltage level reference node; and

a fifth p-channel transistor with a first source/drain region coupled to the gate of the fourth p-channel transistor, a second source/drain region coupled to the third reference voltage node, and a gate coupled to first source/drain region of the fourth p-channel transistor.

15. The circuit of claim 9 wherein a signal carried at the first enable signal node is an inverted version of a signal carried at the second enable signal node.

16. The circuit of claim 9 and further comprising an inverter coupled between the first enable signal node and the second enable signal node, the inverter including a level shifting circuit.

17. The circuit of claim 16 wherein the inverter includes an input coupled to the first enable signal node and an output coupled to the second enable signal node.

18. The circuit of claim 9 wherein the third voltage level is greater than the first voltage level.

19. The circuit of claim 16 wherein the third voltage level is 2.5 volts and the first voltage level is 2.1 volts.

20. A level shifting circuit comprising:

a level-shifting section responsive to an input logic signal, the input logic signal varying between a first voltage level and a second voltage level, the level-shifting section providing an

output logic signal at an output terminal thereof, the output logic signal varying between the first voltage level and a third voltage level, the third voltage level being different than the second voltage level;

a first reference voltage node carrying a voltage at the first voltage level;

a third reference voltage node carrying a voltage at the third voltage level; and

an enable/disable section including a first portion coupled between the level shifting section and the first reference voltage node and a second portion coupled between the level shifting section and the third reference voltage node, the enable/disable section being responsive to an enable/disable signal, the enable/disable section causing the output terminal to be placed at a relatively high output impedance condition independent of the logic state of the input logic signal in response to a disable mode indication from the enable/disable signal.

21. The circuit of claim 20 wherein the first voltage level and the third voltage levels are representative of a first logic state and wherein the second voltage level is representative of a second logic state.

22. The circuit of claim 20 wherein the level-shifting section comprises:

a first transistor with a current path coupled between the third reference voltage node and the output terminal; and

a second transistor with a current path coupled between the output terminal and the first reference voltage node.

23. (Amended) The circuit of claim 22 wherein the enable/disable section comprises:

a third transistor with a current path coupled in series the current path of the first transistor, the current path of the third transistor coupled between the third reference voltage node and the first transistor; and

a fourth transistor with a current path coupled in series the current path of the second transistor, the current path of the fourth transistor coupled between the first reference voltage node and the second transistor.

24. The circuit of claim 23 wherein both the third and fourth transistors are rendered conductive when the enable/disable signal indicates that the level shifting circuit is in an enable mode and wherein both the third and fourth transistors are rendered non-conductive when the enable/disable signal indicates that the level shifting circuit is in the disable mode.

25. The circuit of claim 20 wherein the first portion of the enable/disable section comprises a first switch between the level shifting section and the first reference voltage node and wherein the second portion of the enable/disable section includes a second switch coupled between the level shifting second and the third reference voltage node.

26. The circuit of claim 25 and further comprising an inverter coupled between a control terminal of the first switch and a control terminal of the second switch.

27. The circuit of claim 26 wherein the inverter includes an input coupled to the control terminal of the first switch and an output coupled to the control terminal of the second switch.

28. The circuit of claim 26 wherein the inverter is coupled to the third reference voltage node.

29. The circuit of claim 28 wherein the inverter includes a level shifter coupled to the third reference voltage node and to a voltage node at the first voltage level.

30. The circuit of claim 25 wherein the first and second switches comprise MOS transistors.